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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/743,113	12/22/2003	Kyung Yun Jung	SUN-DA-114T	8491

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EXAMINER	
MONDT, JOHANNES P	

ART UNIT	PAPER NUMBER
3663	

MAIL DATE	DELIVERY MODE
06/25/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/743,113	JUNG, KYUNG YUN	
	Examiner	Art Unit	
	JOHANNES P. MONDT	3663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 March 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Amendment filed on 3/11/08 forms the basis for this office action. In said Amendment applicant amended claims 1, 2 and 4-6. Applicant also amended the Specification and submitted Replacement Sheets for Drawings of Figures 4, 5C and 4D.

Comments on "Remarks" submitted with said Amendment are included below under "Response to Arguments".

Response to Arguments

1. Applicant's arguments filed as Remarks with said Amendment have been fully considered but they are not persuasive. In particular, applicant exaggerates what is needed from Wei, which is only the coverage "by an insulating layer blanket deposited over all" (col. 3, l. 20+ and Figure 7), which teaching, when applied to Tung et al enlarges the insulating layer beyond merely insulating layer 30, fully embedding the entire structure 42 therein. Thereby, as pointed out in the Non-Final Office Action mailed 12/11/07, rendering said insulating layer blanket deposited together with insulating layer 30 to be interpretable as "second insulating layer". See page 9 of said Office Action.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. ***Claims 1-10*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukuzumi (JP 2002-334928) (a computerized translation from the JPO is referred to), in view of X.

Fukuzumi teaches a semiconductor device (title), comprising:

a capacitor having a bottom electrode (channel when gate electrode 14 causes the ON state) (for gate electrode see Figure 3 and "Description of Drawings"), a dielectric layer formed on the bottom electrode (gate dielectric 13; see "Description of Drawings"), and an upper electrode 14 formed on the dielectric layer (see "Description of the Drawings") [Examiner note: thus forming a MOS or MIS capacitor], the capacitor being formed on a semiconductor substrate 10 (see Abstract);

a first insulating layer 18 formed on the semiconductor substrate to cover the capacitor (see "Description of Drawings" and Drawing 3);

a plurality of first contact plugs (23, 23a) formed in a plurality of first via holes of the first insulating layer (see Drawing 3, Abstract; and "Description of the Drawings"), each of the plurality of first contact plugs being electrically connected to either the bottom (23 connected to channel) or upper (23a to gate electrode);

a first metal wiring (horizontal bottom portion of 25; Drawing 3 and Abstract) formed on the first insulating layer and connected to the bottom electrode through one of the first contact plugs;

a second contact plug (any of two upwardly oriented legs of 25; Drawing 3 and "Description of Drawings") in the second insulating layer formed on the first insulating

layer and connected to the upper electrode through another one of the first contact plugs;

an anti-fuse 26 (Abstract, par. [030] and Drawing 3) formed on the second contact plug in a second via hole of the second insulating layer capable of being used (depending on applied voltage) for electrical connection of a third contact plug (narrow lower portion of 30: see Abstract and Drawing 3) to the second contact plug;

the third contact plug filling the second via hole and formed within the anti-fuse (Examiner note: the narrow lower portion of 30 is "within" 26 because a straight line can be drawn connecting points of 26 that intersects with said lower narrow portion of 30: see Drawing 3); and

a second wiring (upper wider portion of 30) formed on the second insulating layer and electrically connected to the third contact plug and the anti-fuse (through the lower, narrower portion of 30) (see Drawing 3 and Description of the Drawings).

Fukuzumi does not necessarily teach the limitation that "the third contact plug does not directly contact the second insulating layer". It is noted, however, that Fukuzumi does teach the desirability of low resistance of the anti-fuse structure (see computerized translation, par. [054]). However, it would have been obvious to include said limitation in view of Cooney, III et al, who, in a patent on interconnects in integrated circuits, hence analogous art, teach a barrier layer 3 to prevent contact between a low-resistance copper comprising contact plug 1 and its surrounding insulating layer 2 (see Figure 1 and col. 2, l. 47 – col. 3, l. 42). The advantages of copper metallization has long been recognized by the entire semiconductor industry (see Cooney III et al, col. 1,

l. 33+), including low resistance (see Cooney et al, col. 1, l. 21-27), on account of which the selection of a copper comprising material as advocated by Cooney III et al would have been obvious in Fukuzumi; however, because copper tends to diffuse into the surrounding insulating material Cooney et al teach the inclusion of a barrier layer 3 preventing contact between the contact plug and the surrounding insulating material (col. 1, l. 47-56).

Motivation to include the teaching by Cooney III et al in the invention by Fukuzumi derives directly from the resulting avoidance of degradation through copper diffusion while the selection of a low resistance copper comprising interconnect directly serves the above-referred-to purpose by Fukuzumi of low resistance.

On claim 2: first and second metal wiring are perpendicular to each other (upper, wider portion of 30 and the horizontal portion of 25 have axes of symmetry perpendicular to each other).

On claims 3 and 8: The device of claim 1 would necessarily have to be formed in order to function. Claim 3 fails to further limit the device of claim 1 other than simply form each of their components, claim 8 further limiting claim 3 only by a limitation already included in claim 1.

On claims 4 and 7: the anti-fuse is formed between the second contact plug (upward leg of 25) and third contact plug (narrow portion of 30) and between the second insulating layer 29 and third contact plug 30 (Examiner note: "between" being met since a line can be drawn from one of the objects the anti-fuse is stated to be in between to the other, said line intersecting said anti-fuse) (see Drawing 3).

On claims 5 and 9: the upper surface of the third contact plug and the upper surface of the second insulating layer are in the same horizontal plane (see Drawing 3) (Examiner note: "upper surface" being the surface along the entire upper main boundary, "being in" not necessarily meaning "partly being out").

On claims 6 and 10: the width of the third contact plug is narrower than the width of the second contact plug (Drawing 3).

Response to Arguments

4. Applicant's arguments, see "Remarks", filed 3/11/08, with respect to the rejection of claims 1-10 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground of rejection is made in view of Fukuzumi (JP 2002-334928 A) and Cooney III, et al. (US 6,339,258 B1).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Lee et al (US 6,861,686 B2).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHANNES P. MONDT whose telephone number is (571)272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Johannes P Mondt/
Primary Examiner, Art Unit 3663